

A Silicon Nanocrystal Tunnel Field Effect Transistor

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In this work, we demonstrate a silicon nanocrystal Field Effect Transistor (ncFET). Its operation is similar to that of a Tunnelling Field Effect Transistor (TFET) with two barriers in series. The tunnelling barriers are fabricated in very thin silicon dioxide and the channel in intrinsic polycrystalline silicon. The absence of doping eliminates the problem of achieving sharp doping profiles at the junctions, which has proven a challenge for large-scale integration and in principle allows scaling down the atomic level. The demonstrated ncFET features a 10^4 on/off current ratio at room temperature, a low 30 pA/ μ m leakage current at a 0.5 V bias, an on-state current on a par with typical all-Si TFETs and bipolar operation with high symmetry. Quantum dot transport spectroscopy is used to assess the band structure and energy levels of the silicon island.

The Complementary Metal–Oxide–Semiconductor (CMOS) technology is at the heart of modern electronic devices.¹ The performance of its fundamental component, the Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET), can be evaluated in terms of on/off output current ratio, off-state leakage current, and subthreshold slope.² However, certain performance characteristics of the MOSFET are intrinsically limited by the physics involved in the device.^{1–3} For example, the thermal activation of carriers imposes a limit on the subthreshold slope, which cannot be inferior to 60 mV/decade.² A promising approach is to take advantage of the exponential dependence of tunnelling current on the width of a barrier to block thermal electrons while enabling a fast transistor turn-on with gate voltage, as it is the case in tunnelling Field Effect Transistors (TFETs)³ or Schottky barrier Field Effect Transistors.⁴ In typical TFETs, a single tunnelling barrier is formed by doping the source, channel and drain to form a p–i–n-like junction.³ However, tight control of the doping profile is challenging because of dopant diffusion problems that prevent forming atomically sharp junctions,⁵ therefore limiting the built-in electric field and the on-state current.⁶

In this work, we fabricated and characterized a transistor made out of an intrinsic silicon nanocrystal contacted by two metallic source/drain electrodes, which we call a nanocrystal Field Effect Transistor (ncFET, Fig. 1a). The switching mechanism relies on the gate-induced modulation of a tunnel barrier in a process very similar to a Schottky barrier FET.⁴ This can, in principle, allow sub-60-mV/decade subthreshold slope and extremely low leakage current. Unlike many previous demonstrations of similar devices with self-assembled quantum dots,^{7–9}

ours is entirely nanofabricated with industry-compatible techniques. The ncFET also differs from Schottky barrier FETs with silicide source/drain^{4,10} by three facts. First, the leads are not made of a silicide but of an elemental metal. Second, the channel is very small in all spatial dimensions and separated from the leads by a thin insulator, which makes it effectively an island. Third, its very flexible fabrication process uses polycrystalline silicon (poly-Si) and differs wildly from planar¹ or silicon-on-insulator^{2,11} MOSFETs. Doping is intentionally avoided to enable extreme scaling of the device dimensions and avoid the dopant diffusion and non-uniformity problems mentioned earlier.

The transistors were fabricated using a nanodamascene process based on the one of Dubuc *et al.*¹² An oxidized silicon substrate is patterned with electron beam lithography and a CF₄/H₂/He Inductively Coupled Plasma (ICP) process¹³ to produce 25 nm wide and 20 nm deep source/drain nanotrench and lateral gate trench. A 40-nm-thick amorphous silicon (a-Si) film is deposited using Low Pressure Chemical Vapor Deposition (LPCVD) at 525 °C. An a-Si nanowire is then patterned over and perpendicular to the nanotrench using a C₄F₈/SF₆ ICP etch.¹⁴ The resulting structure is shown in Fig. 1c. A 800 °C Rapid Thermal Anneal (RTA) is used to form poly-Si with a thin film grain size in the range of 150 to 300 nm with the goal of forming an island with few or no grains. The tunnel junctions are prepared by etching the native oxide at the surface of the poly-Si nanowire using diluted hydrofluoric acid (HF) and letting it re-oxidize for 2 hours in cleanroom air before Ti deposition, which yields an estimated SiO₂ thickness of 0.5 nm. Titanium is deposited and then polished using a Chemical Mechanical Polishing (CMP) process,¹⁵ which isolates the silicon island and yields the structure of Fig. 1d. This key step enables the unique nanocrystal geometry and positioning. Very interestingly, the nanodamascene poly-Si process

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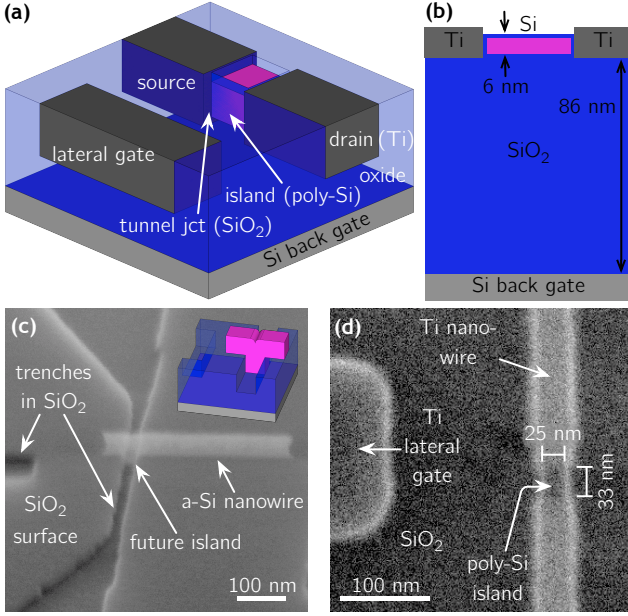


Figure 1. (a) Schematic view of the ncFET (not to scale). (b) Schematic cross-section along the source/drain axis, showing transistor materials stack and actual dimensions. (c) Lateral-view Scanning Electron Microscope (SEM) image of a transistor at an intermediate fabrication step. It shows the source/drain nanotrench, the lateral gate trench and the etched a-Si nanowire overlapping the source/drain trench to form the future transistor island. (d) Top-view SEM image of a finished device. The final CMP step isolates the island after removing all material not embedded in a trench.

opens the door to using different lead and channel materials, as well as integration over various types of substrates.

The transistor characteristics of the ncFET are shown in Fig. 2. Current through all terminals is monitored to validate that source-drain current goes through the island and that gate leakage is always below 0.5 pA and therefore negligible. The substrate is used as a back gate to supply voltage V_G relative to the drain with an oxide thickness of 86 nm. The lateral gate being located 180 nm from the island in the featured device, its contribution is small compared with the back gate and hence is neglected in the following discussion. The channel width is 25 nm.

As shown by the data of Fig. 2a, the transistor is a normally off device and works equally well for positive and negative gate biases. The current rises exponentially with gate bias, a clear sign of tunnelling. This rise shows no indication of saturation for all accessible gate biases. Since the source is a metal, supply of electrons should not be a limiting factor. Moreover, the junction being in principle close to atomically sharp, it can build much bigger electric fields than doped junctions.⁶ Therefore, better gate electrostatics (e.g. lower equivalent oxide thickness and source-gate overlap) are expected to yield significantly better I_{on} ,¹⁶ while the demonstrated value of $2.5 \mu\text{A}/\mu\text{m}$ at $V_{DS} = 0.9 \text{ V}$ and $V_G = 25 \text{ V}$ is already on a par with all-silicon TFETs that do not include CMOS technology

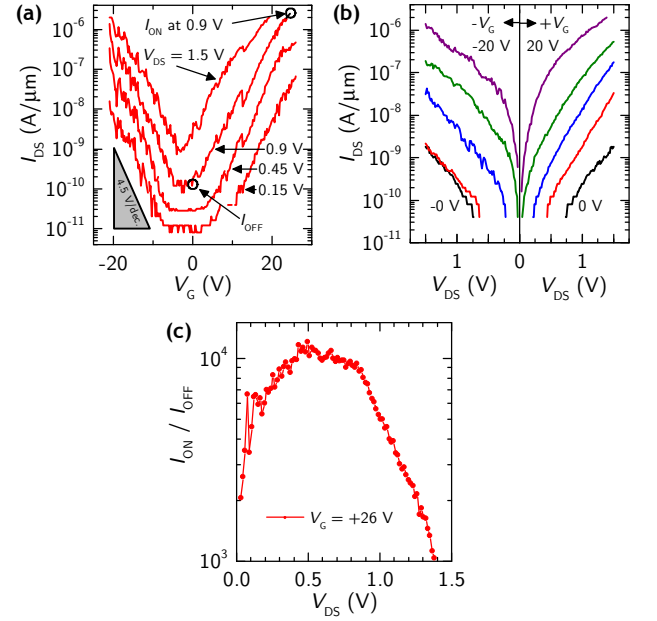


Figure 2. (a) $I_{DS} - V_G$ characteristics for $V_{DS} = 0.15 \text{ V}$, 0.45 V , 0.9 V and 1.5 V showing near-perfect bipolar behavior. The subthreshold slope for this gate geometry is 4500 mV/decade . (b) $I_{DS} - V_{DS}$ characteristics for positive and negative values of V_G (5 V intervals). (c) Demonstrated on/off current ratio as a function of V_{DS} . The I_{on} and I_{off} values are taken from (a) at $V_G = +26 \text{ V}$ and 0 V , respectively. The ncFET can therefore operate over a wide range of V_{DS} values, making it capable of working at typical ($\sim 1 \text{ V}$) and low-power ($< 0.5 \text{ V}$) supply voltage.

boosters and source-gate overlap.^{3,16} The demonstrated I_{on} and I_{off} are both roughly two orders of magnitude smaller than Schottky barrier FETs.⁴ Taking into account that I_{on} could be further improved to $150 \mu\text{A}/\mu\text{m}$ (see discussion below), the ncFET then compares very favorably with both Schottky barrier FETs⁴ and optimized all-silicon TFETs.^{3,16}

A plateau of leakage current is observed at low V_G and V_{DS} (Fig. 2a). Possible leakage mechanisms are thermionic emission over the barrier,⁶ Shockley-Read-Hall generation⁶ at the lead-island interface, and direct or trap-assisted tunnelling through the island.⁶ Preliminary results at low temperature on similar devices indicate that the leakage plateau is mostly independent of temperature. Therefore, the most likely leakage mechanism is direct and potentially trap-assisted tunnelling. This would also be consistent with the high current noise and will be discussed again later. The leakage current is $120 \text{ pA}/\mu\text{m}$ at $V_{DS} = 0.9 \text{ V}$. This is 40 times smaller than low operating power MOSFETs and 830 times smaller than high performance MOSFETs.¹⁷ The leakage current (extracted from Fig. 2a at $V_G = 0 \text{ V}$) reduces to $30 \text{ pA}/\mu\text{m}$ at a lower $V_{DS} = 0.45 \text{ V}$ value, which is the projected low-operating-power supply voltage.¹⁷

An important parameter is the I_{on}/I_{off} ratio. From the graph of Fig. 2c, it is seen that I_{on}/I_{off} is maintained

well above 10^3 over a wide range of V_{DS} values, from 0 V to 1.5 V, and reaches 1.2×10^4 . This makes the ncFET a very versatile device able to operate both at high and low supply voltage. While improving I_{off} would require a longer channel or an improved processing, I_{on} can be easily enhanced. In fact, redesigning the interconnect circuit could allow to push the gate swing to 30 V, improving I_{on}/I_{off} to an extrapolated value of 10^6 by increasing I_{on} to $150 \mu\text{A}/\mu\text{m}$, enough to start competing directly with the one of MOSFETs.^{3,17} Such a high I_{on} has already been achieved using a more favorable gate configuration.¹⁸ Moreover, adding a state-of-the-art high-k dielectric gate stack could reduce the equivalent oxide thickness from 86 nm to below 1 nm. This would correspond to a scaling of the gate voltage from 30 V to 0.35 V and of the subthreshold slope from 4500 mV/decade to below 52 mV/decade, making it useful for low-power applications.

We now investigate the similarity of the structure with quantum dots. This is motivated by the geometry of the device, which is expected to trap electrons inside the channel due to the thin oxide layer in the tunnel junction. In fact, quantum dot transport spectroscopy can provide us with insights on the band structure of the channel or island and help understand the transport mechanisms. In the quantum dot picture, the energy states of the electrons in the island are discrete due to the charging energy E_C and quantum confinement energy E_K .¹⁹ The energy required to add an electron onto the island is then $E_{add} = E_C + E_K$. A transport spectroscopy measurement can allow to identify these energy levels.²⁰ It consists of a measurement of I_{DS} as a function of both V_{DS} and V_G . The diamond-shaped regions of blocked current, called Coulomb diamonds, contain the information on the energy level structure of the island. Figure 3a shows such a measurement, where a wide, diamond-shaped region of blocked current appears in the center of the plot. In our structure, the silicon gap appears as a large gap between the energy levels of the valence and conduction bands (Fig. 3f). If the temperature is higher than the small intraband levels, but much smaller than the gap, we then expect to see one large Coulomb diamond with an addition energy approximately equal to the silicon gap 1.12 eV.¹ Our data does agree with this model. From Fig. 3a (black dashed line), we extract an addition energy of 1.3 eV, close but larger than the gap value. It is suspected that the difference could be accounted for by the very small dimension of the island in the vertical direction (around 5 to 7 nm), where quantum confinement causes an increase in bandgap.²¹ The high symmetry between positive and negative values of V_G is a strong indication that the band alignment of Fig. 3f is experimentally correct. This allows us to describe qualitatively the band structure for different configurations of V_{DS} and V_G . For example, the diagram of Fig. 3c illustrates the main leakage mechanism at high V_{DS} . When gate bias is applied (Fig. 3b or 3d), the bands are curved up or down, allowing to modulate the width of the tunnelling barrier. The electrostatic screening from

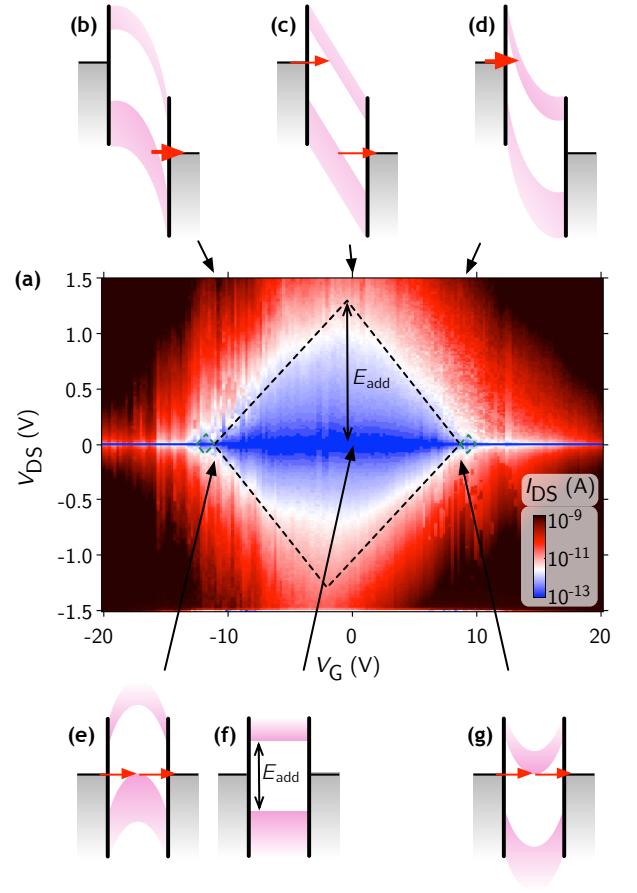


Figure 3. (a) Transport spectroscopy at 300 K showing features similar to Coulomb blockade (black dotted line). Here, the current is plotted in a logarithmic scale as a function of both V_{DS} and V_G . The large $E_{add} = 1.3$ eV is caused by the silicon bandgap, enlarged from its bulk value 1.12 eV by strong quantum confinement in the vertical direction. Note that the current is not per unit gate width. (b–g) Band edge schematic for different values of gate voltage and source–drain bias. Diagrams are approximately to scale. The thick vertical black line represents the thin SiO_2 barrier. (f) Neutral band alignment, showing the slightly enlarged silicon bandgap. (e, g) At low V_{DS} , the gate attracts electrons (g) or holes (e) onto the island. The large quantum confinement energy causes additional hundred meV, ill-defined, room-temperature Coulomb diamonds (green dotted lines). (c) Leakage mechanism where electrons can tunnel through the island even in the absence of gate bias due to the small island length. (b, d) Gate bias changes the tunnel barrier width, allowing to maintain good I_{on}/I_{off} even at high V_{DS} .

the leads causes the gate to have more influence on the center of the channel than on its ends. This causes a band curvature like the one of Fig. 3e and 3g. Screening effects by the electrons in the channel are neglected, because they are expected to change only the quantitative behavior of the bands. In fact, in these bias configurations, the island is expected to form a potential well that would confine electrons or holes and produce Coulomb blockade at a

lower temperature.²² Indeed, the features observed at low V_{DS} of Fig. 3a (green dashed lines) could be attributed to poorly confined and/or temperature-blurred Coulomb blockade.

From the data of Fig. 2a and 3a, it is seen that the noise level is very high and sometimes telegraphic in nature (not shown). Moreover, charge jumps are visible in the diamond of Fig. 3a. It is suspected that the number of charge defects is large, producing charge fluctuators^{23,24} or trap states that can affect the tunnel junctions. Because the tunnelling transport mechanism is extremely sensitive to distance, any small variation in the device's electrostatic environment is transduced in large current fluctuations. It is unclear whether the defects are located in the surrounding dielectric, the SiO_2 tunnel barrier or the island itself. Nevertheless, we do think that an anneal of the SiO_2 tunnel junction would be beneficial. It should be added that it is expected that the titanium of the leads will consume part of the tunnel junction over time. This process can lead to traps in the barrier and time-evolving behavior. In the future, replacing the SiO_2 and leads materials should be considered.

In summary, we have fabricated a tunnelling field effect transistor with metallic source and drain where the channel is made of a silicon nanocrystal. This transistor relies on intrinsic material for its operation, therefore eliminating the need for doping and allowing aggressive scaling down to the atomic level. Electronic transport is found to occur via tunnelling from the metal source to the channel conduction band at positive gate bias due to the strong electric field achieved in the absence of doping. A relatively good on/off current ratio, reaching 10^4 , is demonstrated at room temperature over a wide range of source-drain bias. We argue that this could be improved to 10^6 with better gate electrostatics. Quantum dot transport spectroscopy was used to assess the band structure and energy levels of the silicon island. It shows that the ncFET could potentially be used as a single electron transistor and trap single electrons or holes. Future investigations will address the details of the transport mechanisms through low temperature transport measurements.

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